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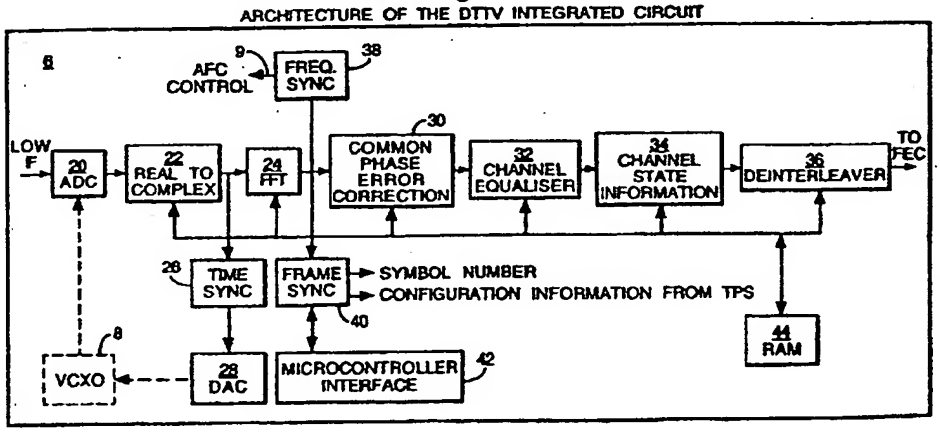
(54) Abstract Title
Demodulating digital video broadcast siginals

(57) A demodulator suitable for implementation in a single chip for demodulating digital video broadcast signals comprising data modulated on a multiplicity of spaced carrier frequencies, wherein an input broadcast signal is converted to a frequency sufficiently low to enable analog digital conversion of the signal, the demodulator comprising analog to digital conversion means (20) for converting the broadcast signal to a series of digital samples, real to complex conversion means (22) for converting each digital sample to a complex number value, Fourier transform means (24) for analysing the complex number values to provide a series of signal values for each carrier frequency, frequency control means (9, 38), comprising means responsive to the output of said Fourier Transform means for producing a signal for controlling the frequency of the signal formed by said complex number values, and signal processing means for receiving the signal values and providing an output for decoding, the signal processing means including channel equalisation means (32) and channel state information generating means (34).

Fig.2.



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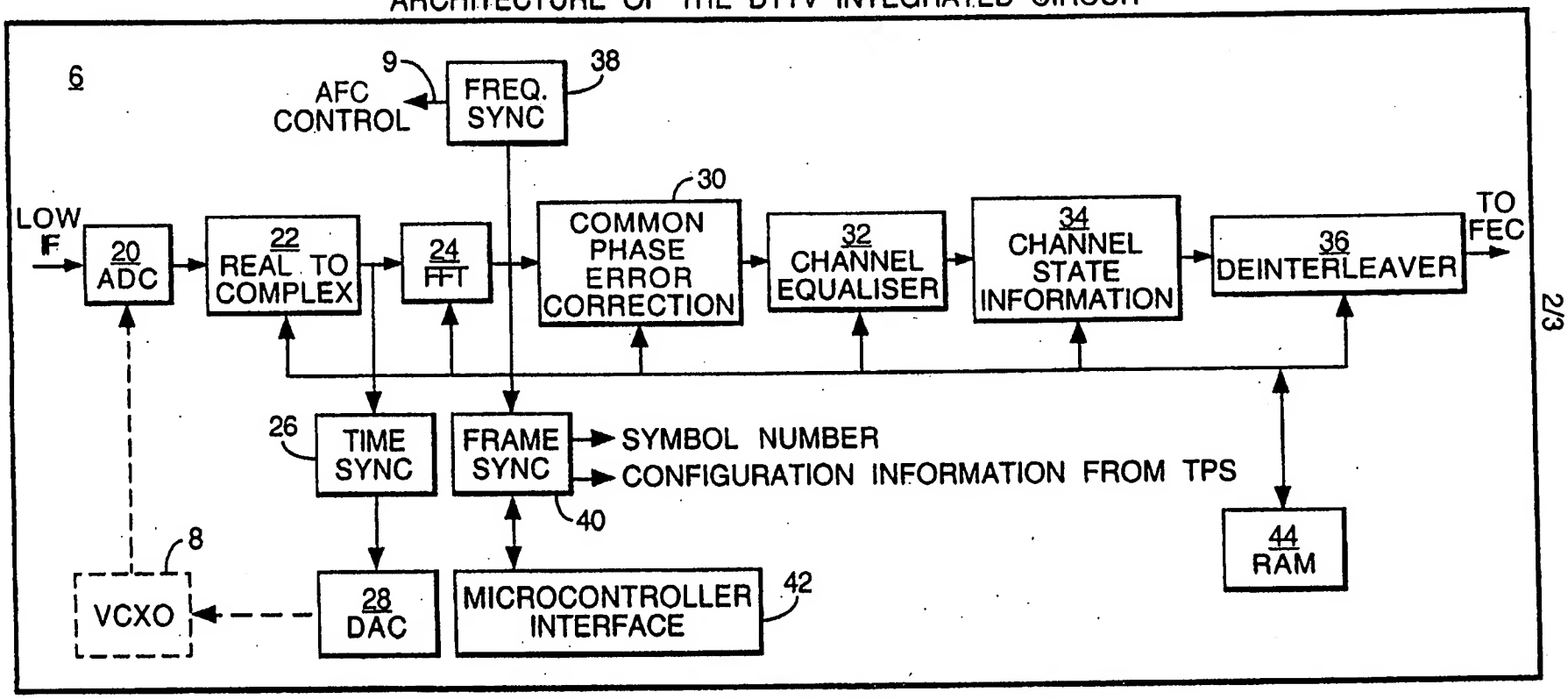
At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

Fig.2.

ARCHITECTURE OF THE DTTV INTEGRATED CIRCUIT



DEMODULATING DIGITAL VIDEO BROADCAST SIGNALS

This invention relates to demodulating digital video broadcast (DVB) signals.

There are currently two major types of DVB, namely, terrestrial broadcasting and satellite/cable broadcasting. The invention is particularly, though not exclusively concerned with terrestrial broadcasting, which has special problems, particularly in communication channel impairment, arising from adjacent television channels, multipath, and co-channel interference, for example. A type of transmission which has been developed to meet these problems is known as Coded Orthogonal Frequency Division Multiplexing (COFDM) - see for example "Explaining Some of the Magic of COFDM" Stott, J.H. - Proceedings of 20th International Television Symposium, Montreux, June 1997. In COFDM, transmitted data is transmitted over a large number of carrier frequencies (1705 or 6817 for DVB), spaced (by the inverse of the active symbol period) so as to be orthogonal with each other; the data is convolutionally coded, to enable soft-decision (Viterbi) decoding. Metrics for COFDM are more complex than those of single frequency networks in that they include Channel State Information (CSI) which represents the degree of confidence in each carrier for reliably transmitting data.

Modulation and Demodulation of the carriers may be carried out by a Fast Fourier Transform (FFT) algorithm performing Discrete Fourier Transform operations. Naturally, various practical problems arise in demodulation, firstly in translating the transmitted signal to a frequency at which demodulation can be carried out, and secondly by accurately demodulating the data from a large number of carriers in a demodulator which is not overly complex or expensive.

It is an object of the present invention to provide a demodulator for digital terrestrial broadcast signals which can demodulate data transmitted by a COFDM system but which may be manufactured simply and inexpensively, preferably in a single integrated circuit chip.

random component and a component which is common to all carriers, arising from local oscillator phase noise. Such common phase error may be removed by a technique as described in more detail below.

The process of demodulation requires very accurate tracking of the input signal and to this end automatic frequency control and timing control are desirable. Timing control is necessary in order to ensure that the timing window for the FFT is correctly positioned in relation to the input waveforms. Thus, the sampling by the ADC must be synchronised with the input wave forms. For an input signal centred on 4.57 MHz, an ADC operating frequency of 18.29 MHz (4.57 x 4) is preferred. The ADC is maintained in synchronisation by a loop control wherein the complex signal value at the input of the FFT is applied to a time synchronisation unit whose output is converted in a digital to analog converter (DAC) to an analog value, which is employed to control a voltage controlled oscillator providing a clock signal to the ADC.

Automatic frequency control (AFC) is necessary to maintain the demodulation process in synchronisation with down-conversion, otherwise a gradually increasing phase error occurs in the recovered signals. To this end, a signal derived subsequent to the FFT, from the demodulated signals may be fed back to the local oscillator for IF generation in order to maintain frequency synchronisation. However, such control has disadvantages of complication in that a control signal must be fed back to the IF generation means and the control signal must adjust the reference crystal within the search range of the AFC. As an alternative therefore, AFC may be provided as a digital control applied to a digital frequency shifter coupled the input of the FFT device. The process of automatic frequency control (AFC) is described in more detail below. However, it will be shown that AFC requires a coarse control and a fine control. The fine control is dependent upon measuring the phase difference (first difference) between two adjacent continual pilot signal samples, whereas the coarse control requires the determination of rate of change of phase (or second difference) i.e., the difference between two consecutive phase differences between adjacent samples.

plurality of delay elements for processing delayed versions of the signal values with the current values, and

wherein the apparatus is arranged such that the phase error correction means employs said first plurality of delay elements in one phase of operation and the channel equalisation means employs said second plurality of delay elements in a different phase of operation whereby to permit the first and second plurality to be constituted by the same memory elements.

BRIEF DESCRIPTION OF THE DRAWINGS

A preferred embodiment of the invention will now be described with reference to the accompanying drawings, in which:-

Figure 1 is a schematic block diagram of a digital terrestrial front end converter incorporating the present invention;

Figure 2 is a more detailed block diagram of demodulating apparatus according to the invention forming part of the converter of figure 1;

Figure 3 is a schematic view of a chip incorporating the apparatus of Figure 2; and

Figure 4 is a schematic block diagram of phase error correction means and channel equalisation means.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The preferred embodiment of the present invention comprises a front end for digital terrestrial television transmitted according to the DVB-T specification. The front end consists of two separate components. First, an analog down-converter that converts the input signal from UHF to a low IF. Second, an integrated circuit chip that accepts the analog signal from the down-converter and performs the required DSP operations, which include synchronisation and demodulation, to form a stream of soft decisions suitable for presentation to an FEC decoder (Forward Error Correction decoder).

Full compliance to the DVB-T specification means that the chip is capable of decoding signals transmitted in the following modes:

voltage controlled oscillator 8, which provides a sampling clock signal to analog to digital converter 20.

The FFT device 24 has four modes of operation. Firstly, it is capable of performing either a 2048 point or an 8192 point transform. Second, it is capable of performing the transform in either direction. The inverse FFT functionality is provided so that the integrated circuit may be used in applications requiring OFDM modulation. In any event, the FFT performs a series of discrete Fourier transforms on each carrier frequency to provide at an output the data symbols for each carrier frequency. These output signals are corrected in phase at a common phase error generator unit 30 and then passed to a channel equaliser 32, a channel state information correction unit 34 and a deinterleaver 36. The signal thus processed is then passed at an output from the demodulator to forward error correction unit 10. The phase error correction block 30 calculates the common phase error of the signal and applies the necessary correction. The channel equaliser 32 first performs linear temporal equalisation followed by frequency equalisation using a high order interpolating filter. The equaliser outputs an equalised constellation to the channel state information unit 34. Unit 34 generates 3 or 4 bit soft decisions which are suitable for presentation to a Viterbi decoder. Deinterleaver 36 performs firstly symbol deinterleaving followed by bit deinterleaving.

In addition, the output signals from FFT 24 are passed to a frequency synchronisation unit 38 which converts it to a control signal for automatic frequency control, which acts upon a local oscillator in down-converter unit 2 for adjusting the frequency of the first or second IF.

In addition, the output of FFT 24 is fed to a frame synchronisation unit 40 whose outputs are fed forward to units 10, 12 and 14 (Fig. 1). A microcontroller interface 42 is provided, and in addition RAM memory 44 is provided to which all the units 22, 24, 30-36 have access to in order to provide their required operations.

Channel Impairments

3) The synthesiser phase-noise characteristics must be compatible with 64-QAM operation.

Memory Budget

A significant problem for demodulator integrated circuit 6 is the amount of RAM 42 that the chip requires.

Architecture component	% RAM
Timing synchronisation	2%
Frequency synchronisation	11%
FFT	38%
Common phase error correction	11%
Channel equalisation	23%
Channel State Information	3%
Deinterleaver	12%

TABLE 1 - Proportion of RAM used

It is necessary to make the best possible use of the RAM. Some of the blocks of memory, such as the FFT and symbol deinterleaver, require fixed amounts of RAM and it is not possible to reduce them (except by reducing the word widths and so degrading the performance). Other blocks, for example, the timing synchronisation, required some algorithmic alterations for the sole purpose of reducing the amount of memory but without degrading the performance. A technique that is employed to make best use of the available memory is to "reuse" some of the memories. For example, the data delay required to implement common-phase-error correction doubles as the first data delay in the channel equaliser. This means that only two additional data delays were required to implement full linear temporal equalisation. This is explained in more detail below with reference to Figure 4.

Table 1 shows the final allocations of RAM that were made in the chip. As this table shows, the highest memory usage is in the FFT circuitry and the smallest is in the

frequency selective fading. The purpose of the channel equaliser 32 is to rotate and scale the constellation so that the constellations on all the carriers are of a known size (but not necessarily of the same reliability). the process is performed by using the scattered pilot information contained in the COFDM signal. The scattered pilots provide a reference signal of known amplitude and phase on every third OFDM carrier. Since this scattered pilot information is subject is subject to the same channel impairments as the data carriers, the scattered pilots are noisy.

In the present invention, temporal linear interpolation is performed between two received scattered pilots, and these interpolated values are used as the reference for frequency equalisation of the data. Since scattered pilots at the same time duration are spaced 4 OFDM symbols apart, a compensating data delay of 3 OFDM symbols must be provided to permit this option.

Common Phase Error Correction versus Down Converter Performance

The down converter performance has a different set of requirements from those demanded by down-converters suitable for analog television. For example, in a down-converter for analogue television, particular attention must be given to the group delay-characteristics. However COFDM has been specially designed to be robust to this type of distortion, and so the group delay is much less important.

Another difference between the two requirements is in the local oscillator phase noise performance. The addition of local oscillator phase noise to an OFDM signal has two principal effects:

1) To rotate the received constellation by an amount which is the same for all carriers within one OFDM symbol, but varying randomly from symbol to symbol. This is called the common phase error (CPE) and primarily results from the lower- frequency components of the phase- noise spectrum; and

2) To add Inter-Carrier Interference (ICI) of a random character similar to additive thermal noise. ICI primarily results from the higher frequency components of the phase-noise spectrum. ICI cannot be corrected and must be allowed for in the noise budget. It can be kept small in comparison with thermal noise by suitable local oscillator design.

frequency). Signals from the inputs and outputs of delay elements 50, 52 are provided to subtraction circuits in a unit 54 in order to derive phase error signals (first difference). In addition, the difference (second difference) between the phase error signals is determined in unit 56. These phase error signals are averaged for the continual pilot signals, as more particularly described in our copending application (GBP1288A). The assessed common phase error is applied to correction circuits 58, 60 , the output to correction circuit 60 being applied via a further delay element 62. The signal outputs from memory elements 50, 52 are thus corrected for phase in circuits 58, 60, and are applied to an interpolator 66 in channel equaliser circuit 32. The output circuit from correction circuit 58 is applied directly to the interpolator, but the signal from correction circuit 60 is applied to the interpolator firstly directly at tapping 68 and then via first and second memory elements 70, 72. Since the interpolator is provided with three sets of delayed symbols from delay element 62 and memory elements 70, 72 interpolation can be carried out on scattered pilots spaced four symbols apart, as provided in the ETSI standard and as described above.

By arranging for the circuits to operate in two phases of operation, in the first of which the common phase error is computed using delay elements 50, 52, and in the second of which interpolation occurs using memory elements 70, 72, it is possible to provide the two sets of memory elements 50, 52 and 70, 72, from the same section of RAM memory.

5. Apparatus according to any preceding claim, including time synchronisation means for controlling the sampling by the analog to digital conversion means, comprising means responsive to the input signal to the Fourier transform means for providing a signal for controlling a voltage control oscillator for determining the sampling frequency of the analog to digital conversion means.

6. Apparatus according to any preceding claim, wherein said frequency control means, comprises means responsive to the output of said Fourier transform means for providing a signal for controlling local oscillators for said first and/or second IF frequencies.

7. Apparatus according to any of claims 1 to 5, wherein said frequency control means is arranged to provide a digital correction signal for application to the input of said Fourier Transform means.

8. Apparatus according to any preceding claim, including phase-error-correcting means for removing the common phase error in said signal values, including a first plurality of delay elements for processing delayed versions of the signal values with current signal values, and including channel equalisation means for compensating for communication channel impairments for receiving the phase-error-corrected signal values and including a second plurality of delay elements for processing delay versions of the signal values with the current values,

and wherein the apparatus is arranged such that the phase-error-correction means employs said first plurality of delay elements in one phase of operation of the apparatus and the channel equalisation means employs said second plurality of delay elements in a different phase of operation of the apparatus, whereby the first and second pluralities are one and the same.

means including channel equalisation means and channel state information generating means.

11. Apparatus according to claim 9 or 10, incorporated in an integrated circuit chip.

12. A method of demodulating digital video broadcast signals comprising data modulated on a multiplicity of spaced carrier frequencies, the method comprising:

converting an input broadcast signal to a frequency sufficiently low to enable analog to digital conversion of the signal,

converting the broadcast signal to a series of digital samples,

converting each digital sample to a complex number value,

analysing the complex number values to provide a series of Fourier transform signal values for each carrier frequency,

producing a signal from said Fourier Transform signal values for controlling the frequency of the signal formed by said complex number values,

performing channel equalisation on said Fourier Transform signal values,

generating state information from said Fourier Transform signal values and including said state information and channel equalisation in an output for decoding based on said Fourier Transform signal values.

13. A method for demodulating a digital video broadcast signal comprising data modulated on a multiplicity of spaced carrier frequencies, the metod comprising:

analysing a version of the broadcast signal to provide a series of signal values for each of the multiplicity of carrier frequencies,

removing the common phase error in said signal values by phase-error-correction, including processing delayed versions of the signal values with the current signal values,

compensating the phase-error-corrected signal values for communication channel impairments by channel equalisation, including processing delayed versions of the signal values with the current values,

The Patent Office

19

Application No: GB 9809587.0 **Examiner:** Ken Long
Claims searched: 1 to 14 **Date of search:** 1 October 1998

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Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.P): H4P (PAL, PAR, PAQ & PRE)

Int Cl (Ed.6): H04L 27/26

Other: ONLINE : WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A	EP 0795985 A2	NOKIA (page 5 lines 16-31)	None
A	EP 0786888 A2	SAMSUNG (column 6 line 28 to column 8 line 15)	None

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
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